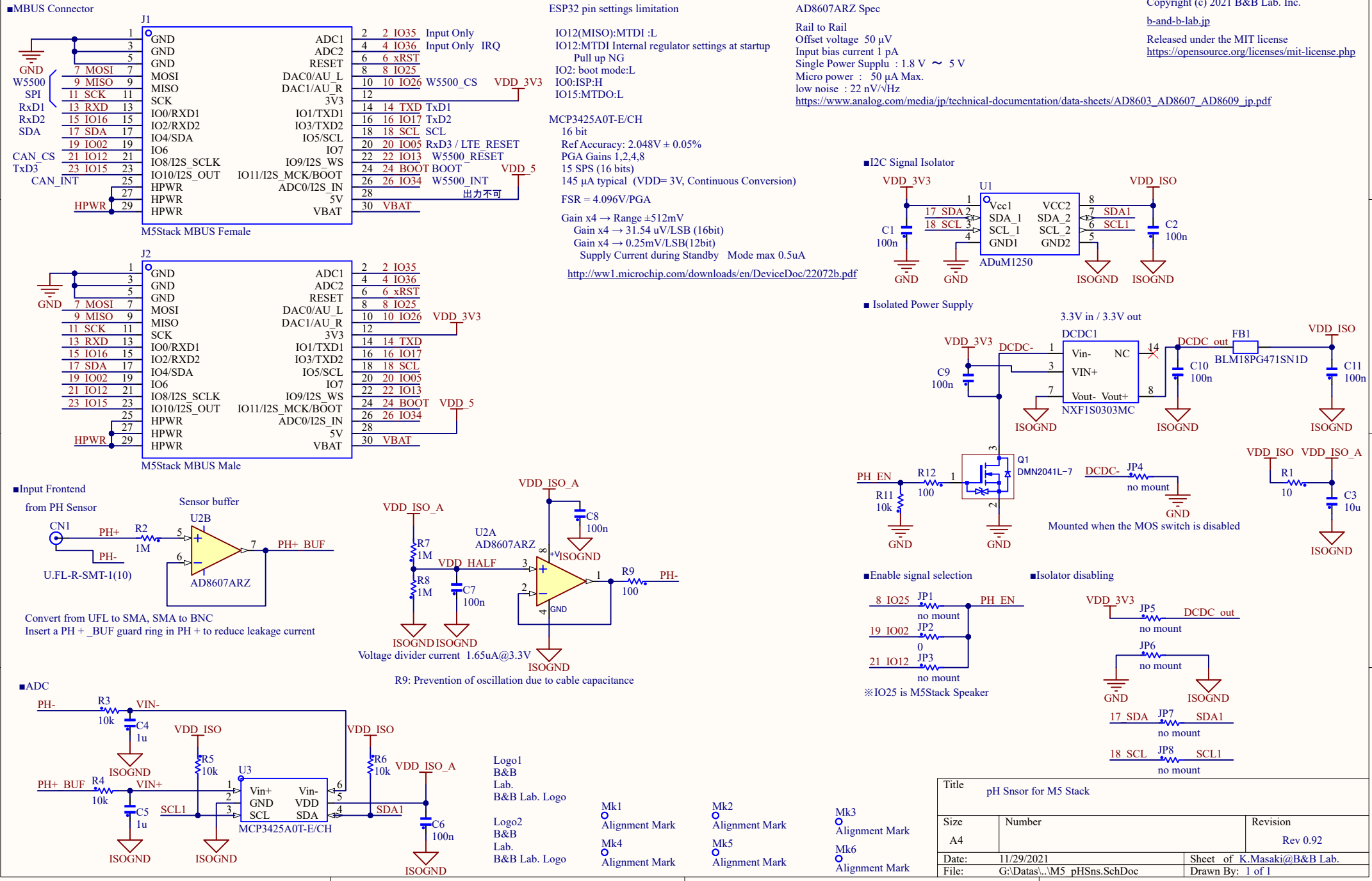
■MBUS Connector
J1
GND
W5500
SPI
RxD1
RxD2
SDA
CAN_CS
TxD3
CAN_INT
HPWR
GND GND GND MOSI MISO SCK IO0/RXD1 IO2/RXD2 IO4/SDA IO6 IO8/I2S_SCLK IO10/I2S_OUT HPWR HPWR HPWR
ADC1 ADC2 RESET DAC0/AU_L DAC1/AU_R 3V3 IO1/TXD1 IO3/TXD2 IO5/SCL IO7 IO9/I2S_WS IO11/I2S_MCK/BOOT ADC0/I2S_IN 5V VBAT
2 IO35 Input Only
4 IO36 Input Only IRQ
6 xRST
8 IO25
10 IO26 W5500_CS
VDD_3V3
14 TXD TxD1
16 IO17 TxD2
18 SCL SCL
20 IO05 RxD3 / LTE_RESET
22 IO13 W5500_RESET
24 BOOT BOOT
VDD_5
26 IO34 W5500_INT
28 出力不可
30 VBAT
M5Stack MBUS Female
J2
GND
HPWR
M5Stack MBUS Male
VDD_3V3
VDD_5
ESP32 pin settings limitation
IO12(MISO):MTDI :L
IO12:MTDI Internal regulator settings at startup
Pull up NG
IO2: boot mode:L
IO0:ISP:H
IO15:MTDO:L
MCP3425A0T-E/CH
16 bit
Ref Accuracy: 2.048V ± 0.05%
PGA Gains 1,2,4,8
15 SPS (16 bits)
145 µA typical (VDD= 3V, Continuous Conversion)
FSR = 4.096V/PGA
Gain x4 → Range ±512mV
Gain x4 → 31.54 uV/LSB (16bit)
Gain x4 → 0.25mV/LSB(12bit)
Supply Current during Standby Mode max 0.5uA
http://ww1.microchip.com/downloads/en/DeviceDoc/22072b.pdf
AD8607ARZ Spec
Rail to Rail
Offset voltage 50 µV
Input bias current 1 pA
Single Power Supplu : 1.8 V ～ 5 V
Micro power : 50 µA Max.
low noise : 22 nV/√Hz
https://www.analog.com/media/jp/technical-documentation/data-sheets/AD8603_AD8607_AD8609_jp.pdf
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■I2C Signal Isolator
VDD_3V3
VDD_ISO
U1
Vcc1 SDA_1 SCL_1 GND1
VCC2 SDA_2 SCL_2 GND2
17 SDA 2
18 SCL 3
7 SDA1
6 SCL1
C1 100n
C2 100n
ADuM1250
GND
ISOGND
■ Isolated Power Supply
3.3V in / 3.3V out
DCDC1
VDD_3V3
DCDC-
Vin- NC
VIN+
Vout- Vout+
NXF1S0303MC
DCDC_out
FB1
BLM18PG471SN1D
VDD_ISO
C9 100n
C10 100n
C11 100n
ISOGND
Q1
DMN2041L-7
PH_EN
R12 100
R11 10k
JP4
no mount
Mounted when the MOS switch is disabled
VDD_ISO_A
R1 10
C3 10u
■Input Frontend
from PH Sensor
Sensor buffer
CN1
PH+
PH-
R2 1M
U2B
AD8607ARZ
PH+_BUF
U.FL-R-SMT-1(10)
Convert from UFL to SMA, SMA to BNC
Insert a PH + _BUF guard ring in PH + to reduce leakage current
VDD_ISO_A
R7 1M
R8 1M
VDD_HALF
C7 100n
U2A
AD8607ARZ
C8 100n
R9 100
PH-
GND
Voltage divider current 1.65uA@3.3V
R9: Prevention of oscillation due to cable capacitance
■Enable signal selection
8 IO25 JP1 no mount PH_EN
19 IO02 JP2 0
21 IO12 JP3 no mount
※IO25 is M5Stack Speaker
■Isolator disabling
VDD_3V3
JP5 no mount DCDC_out
JP6 no mount
17 SDA JP7 SDA1 no mount
18 SCL JP8 SCL1 no mount
■ADC
PH-
R3 10k
VIN-
C4 1u
VDD_ISO
R5 10k
R6 10k
VDD_ISO_A
PH+_BUF
R4 10k
VIN+
C5 1u
SCL1
U3
Vin+ GND SCL
Vin- VDD SDA
MCP3425A0T-E/CH
SDA1
C6 100n
ISOGND
Logo1
B&B
Lab.
B&B Lab. Logo
Logo2
B&B
Lab.
B&B Lab. Logo
Mk1 Alignment Mark
Mk2 Alignment Mark
Mk3 Alignment Mark
Mk4 Alignment Mark
Mk5 Alignment Mark
Mk6 Alignment Mark
Title
pH Snsor for M5 Stack
Size A4
Number
Revision Rev 0.92
Date: 11/29/2021
Sheet of K.Masaki@B&B Lab.
File: G:\Datas\..\M5_pHSns.SchDoc
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